0067075 5776960

FIG. 1

Prior Art

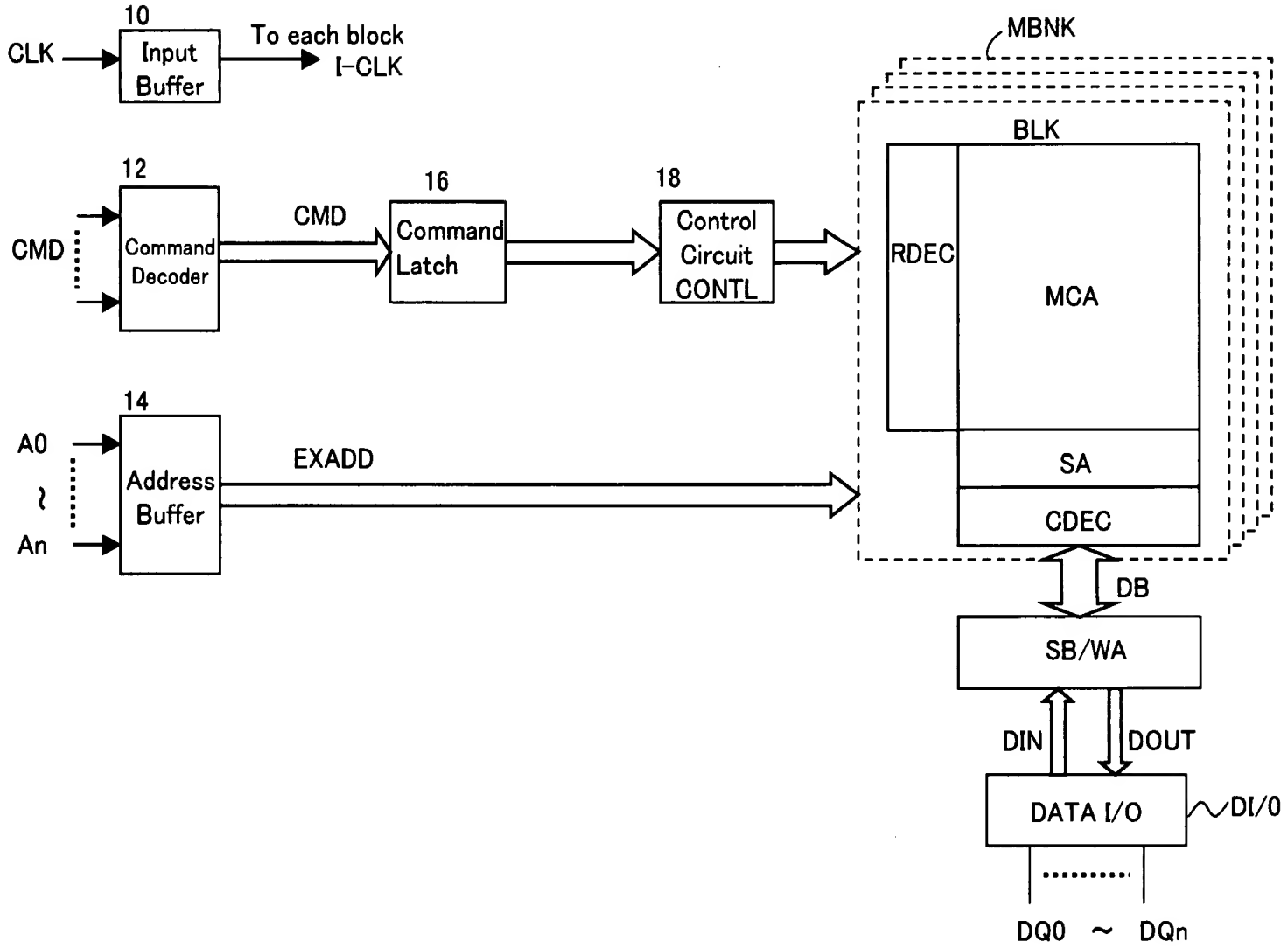


FIG. 2

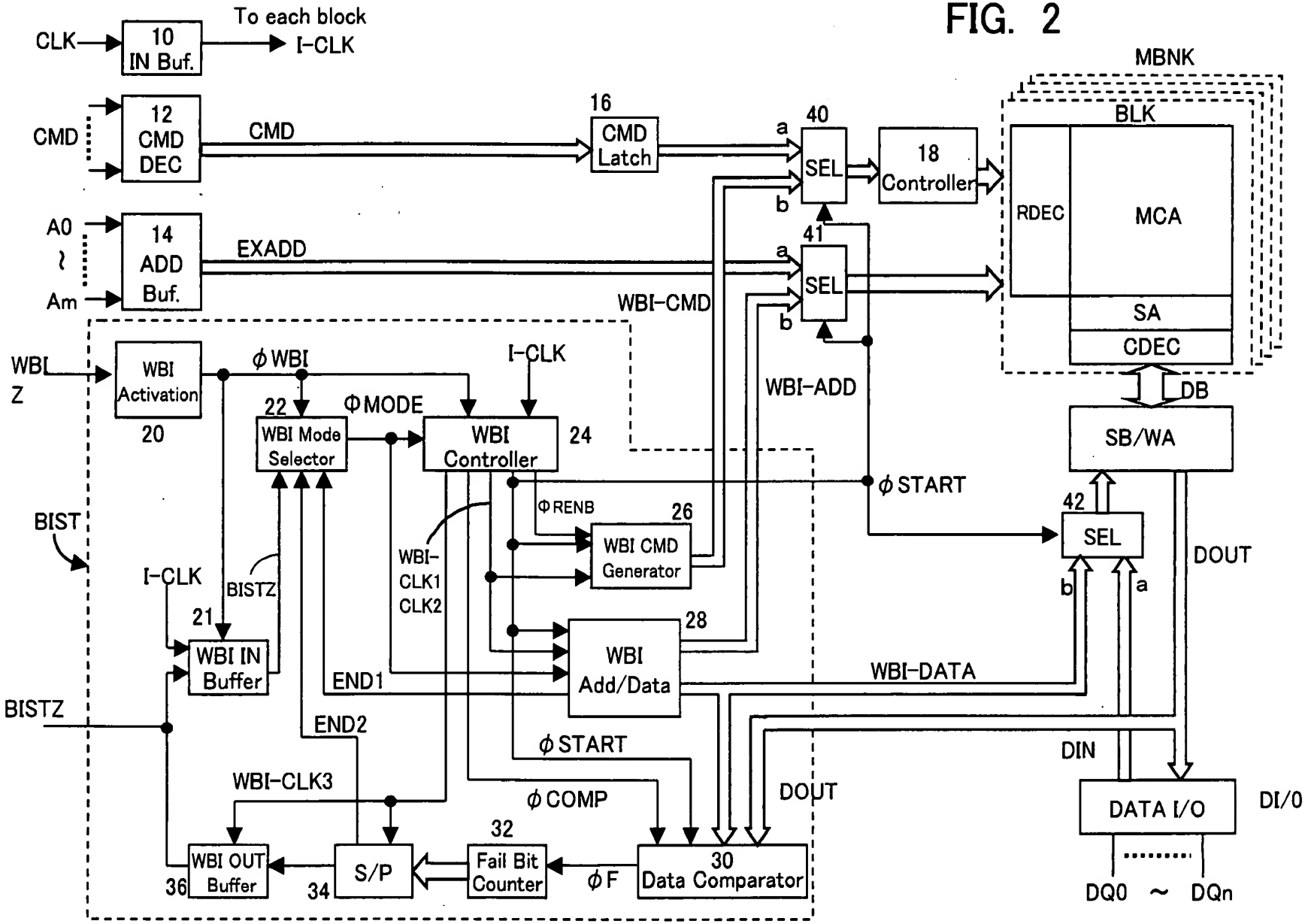

CLK
10
IN Buf.
To each block
I-CLK
CMD
12
CMD
DEC
CMD
16
CMD
Latch
40
a
b
SEL
18
Controller
MBNK
BLK
RDEC
MCA
SA
CDEC
A0
~
Am
14
ADD
Buf.
EXADD
41
a
b
SEL
WBI-CMD
WBI-ADD
DB
SB/WA
WBI
Z
WBI
Activation
20
φWBI
I-CLK
22
ΦMODE
WBI Mode
Selector
WBI
Controller
24
φSTART
ΦRENB
26
WBI CMD
Generator
BIST
I-CLK
BISTZ
21
WBI IN
Buffer
WBI-
CLK1
CLK2
28
WBI
Add/Data
WBI-DATA
42
SEL
b
a
DOUT
END1
BISTZ
END2
φSTART
DIN
WBI-CLK3
φCOMP
DOUT
DATA I/O
DI/0
32
WBI OUT
Buffer
36
S/P
34
Fail Bit
Counter
φF
30
Data Comparator
DQ0 ~ DQn

FIG. 3

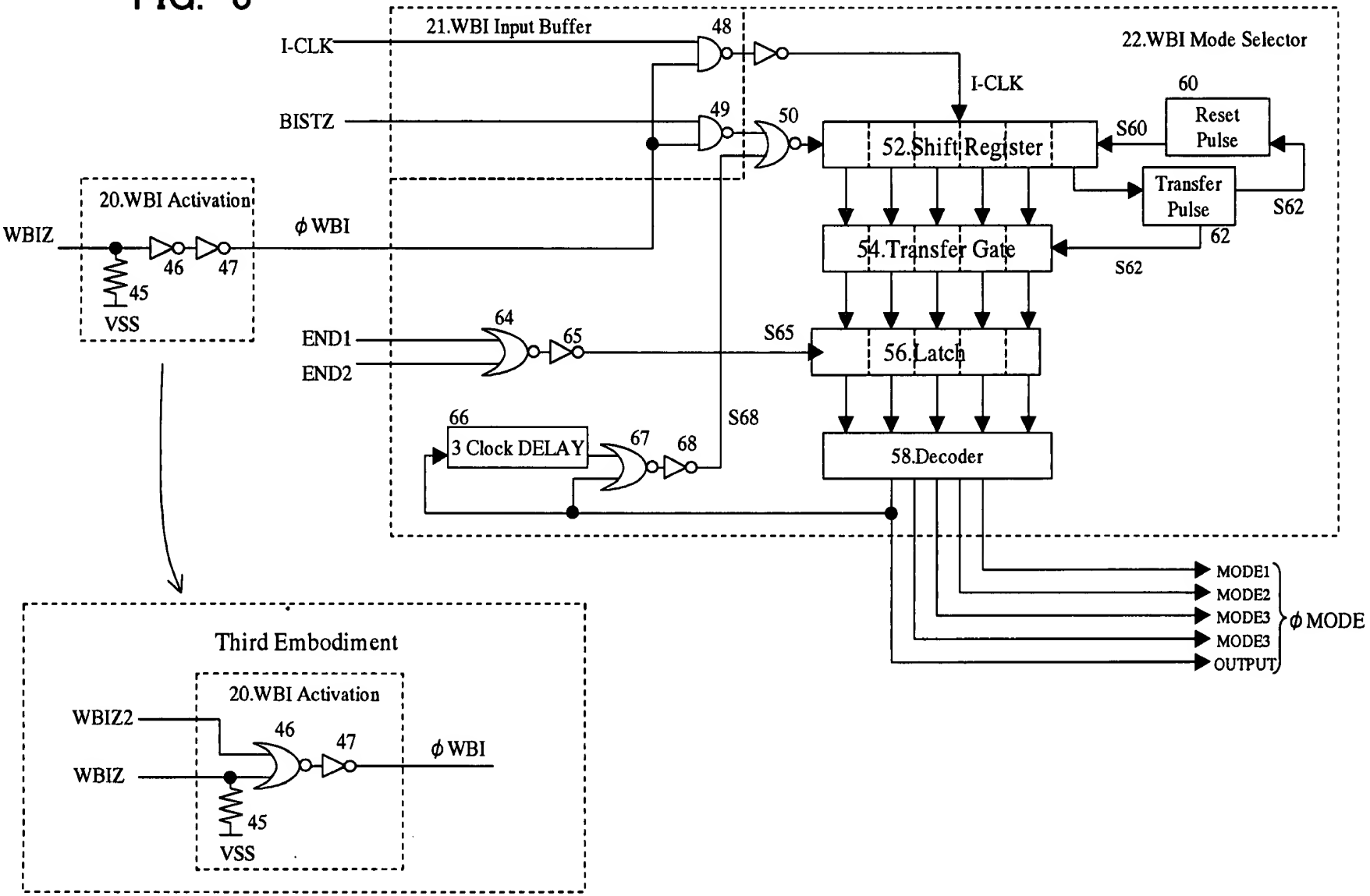
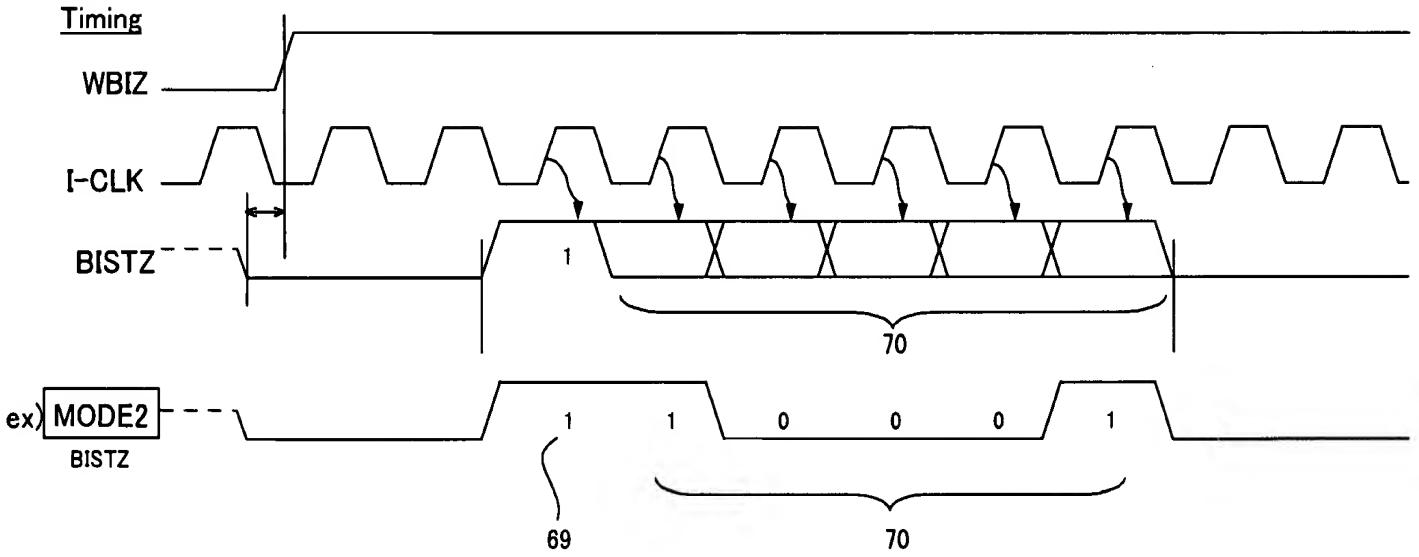
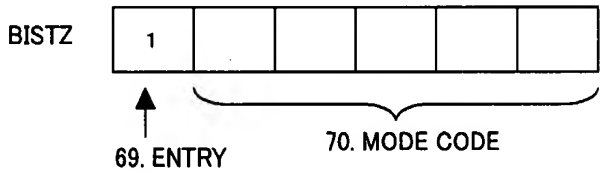

21.WBI Input Buffer
22.WBI Mode Selector
I-CLK
BISTZ
48
49
50
I-CLK
60
Reset Pulse
S60
52.Shift Register
Transfer Pulse
S62
62
54.Transfer Gate
S62
20.WBI Activation
WBIZ
φWBI
46
47
45
VSS
64
65
END1
END2
S65
56.Latch
66
3 Clock DELAY
67
68
S68
58.Decoder
MODE1
MODE2
MODE3
MODE3
OUTPUT
φMODE
Third Embodiment
20.WBI Activation
WBIZ2
WBIZ
46
47
φWBI
45
VSS

FIG. 4





MODE CODE	MODE
10000	MODE1
10001	MODE2
10010	OUTPUT
10011	MODE3
⋮	⋮

FIG. 5

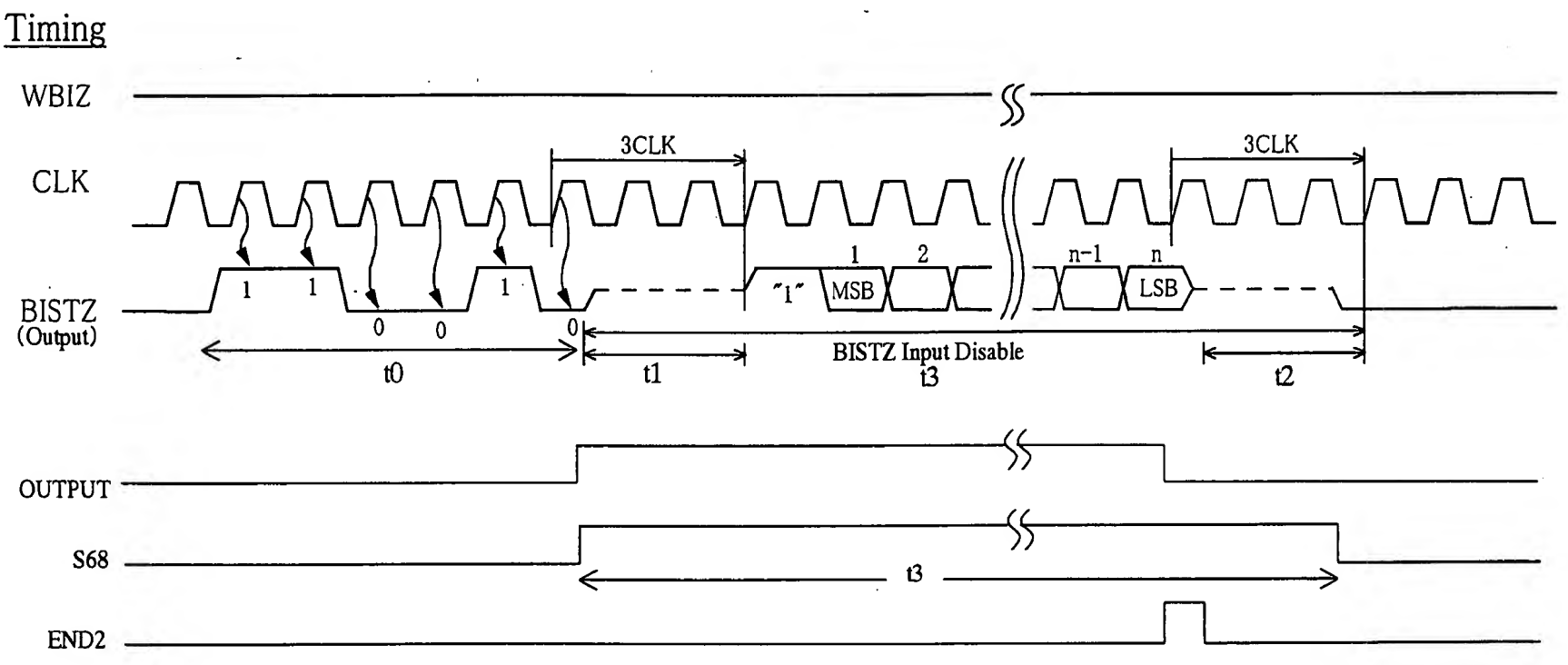

Timing
WBIZ
CLK
3CLK
3CLK
BISTZ
(Output)
1
1
0
0
1
0
1
2
"1"
MSB
n-1
n
LSB
t0
t1
BISTZ Input Disable
t3
t2
OUTPUT
S68
t3
END2

FIG. 6

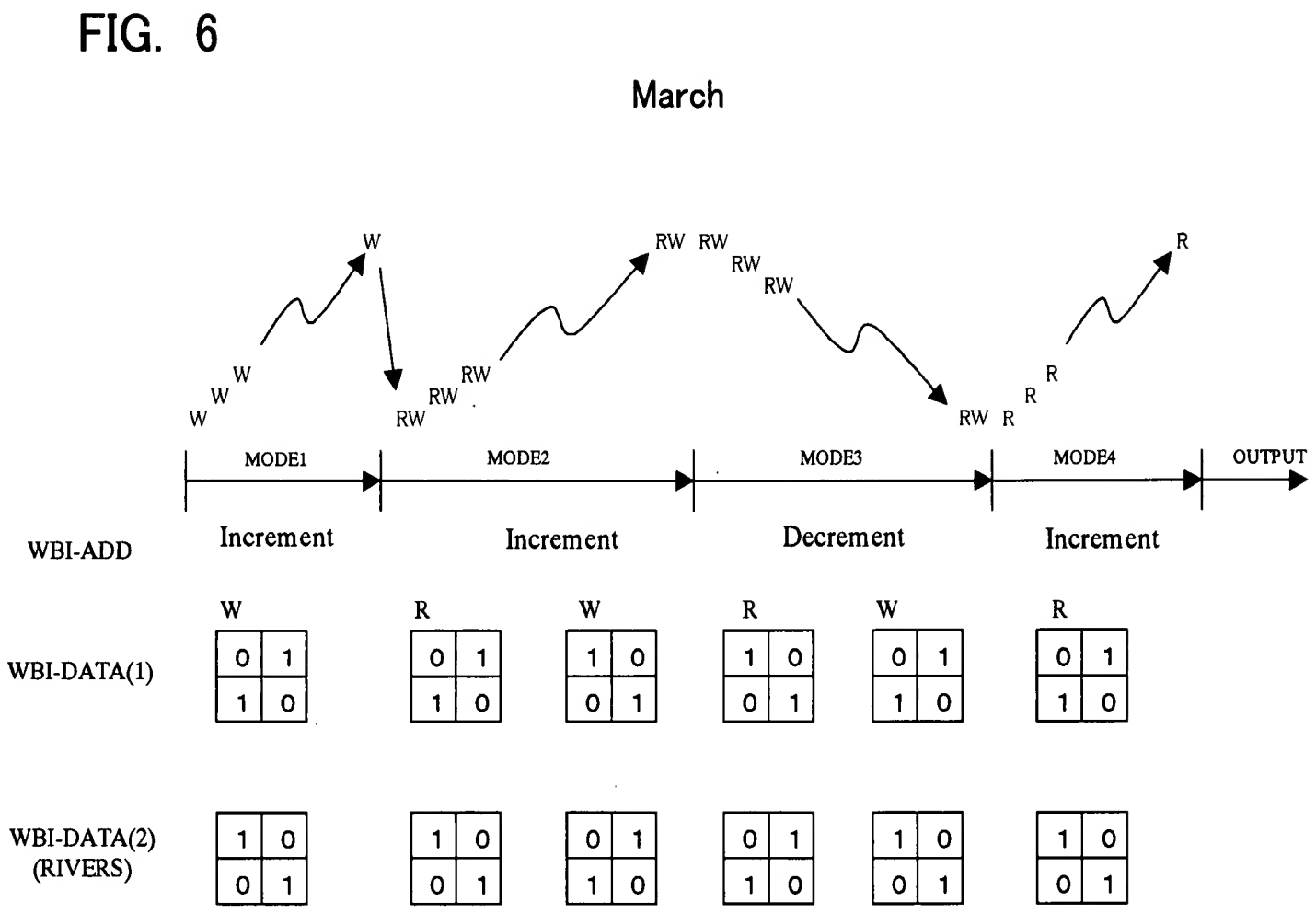

March
W
W
W
W
RW
RW
RW
RW
RW
RW
RW
RW
R
R
R
MODE1
MODE2
MODE3
MODE4
OUTPUT
WBI-ADD
Increment
Increment
Decrement
Increment
WBI-DATA(1)
WBI-DATA(2)
(RIVERS)

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FIG. 7

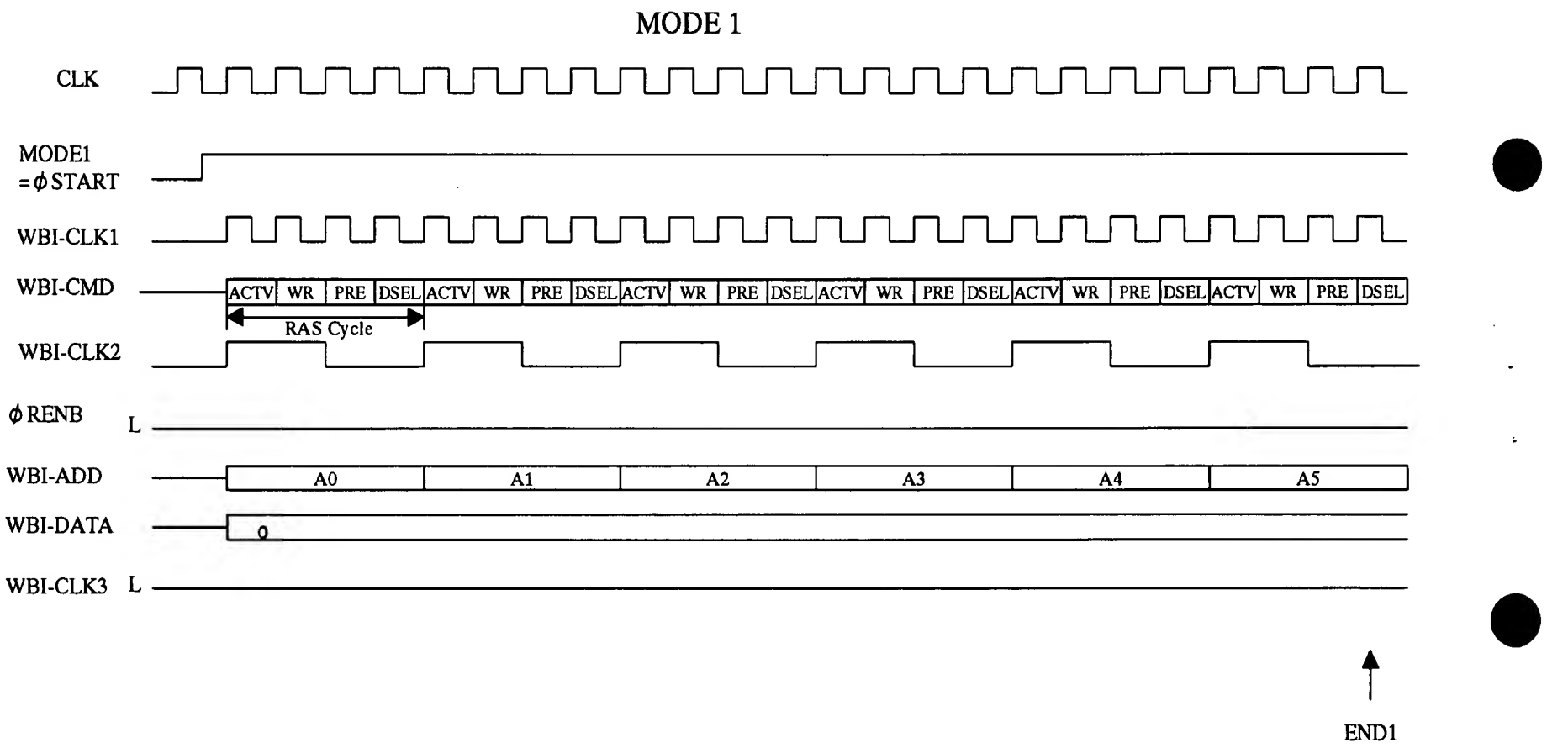

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FIG. 8

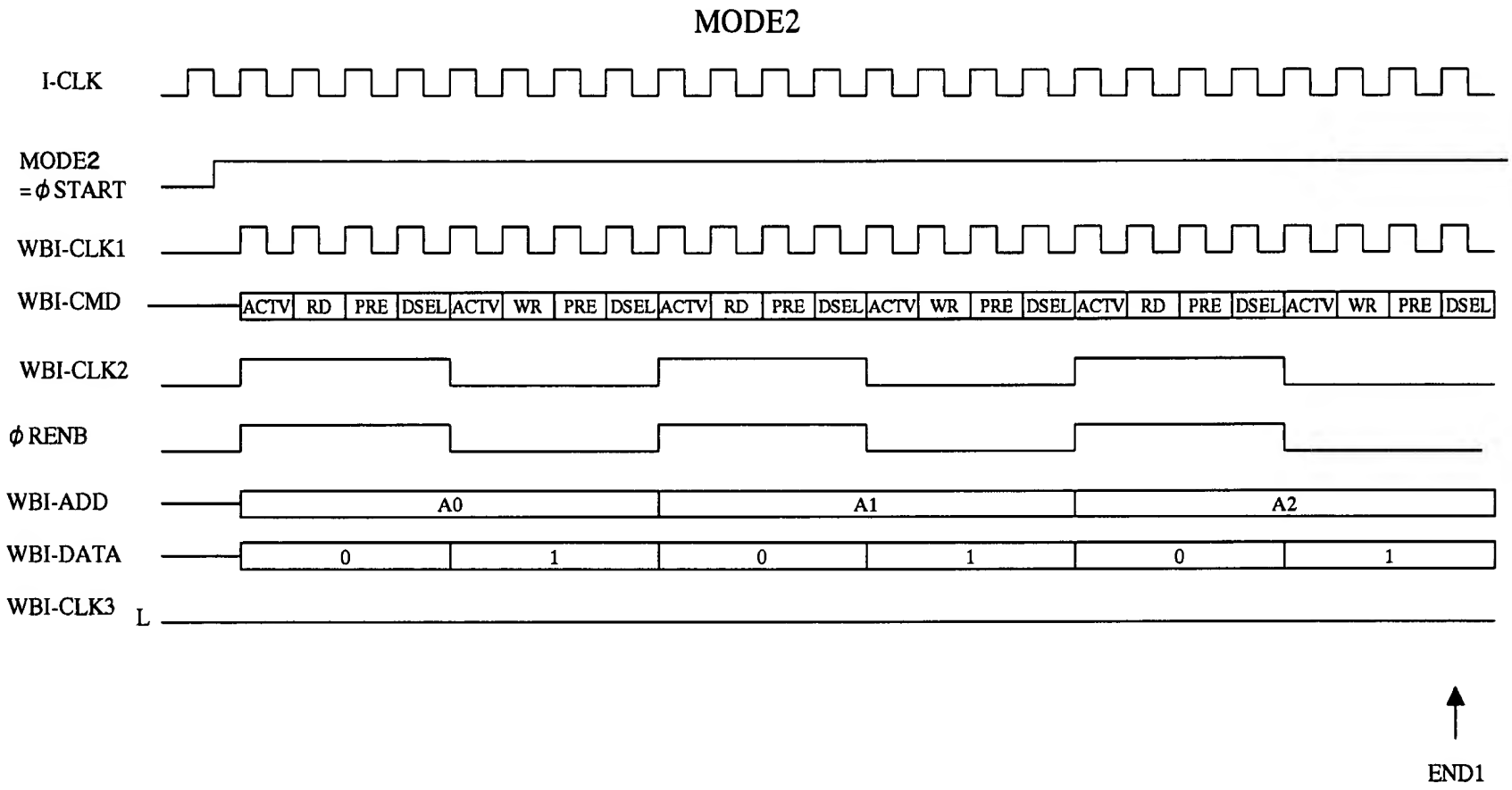

FIG. 9

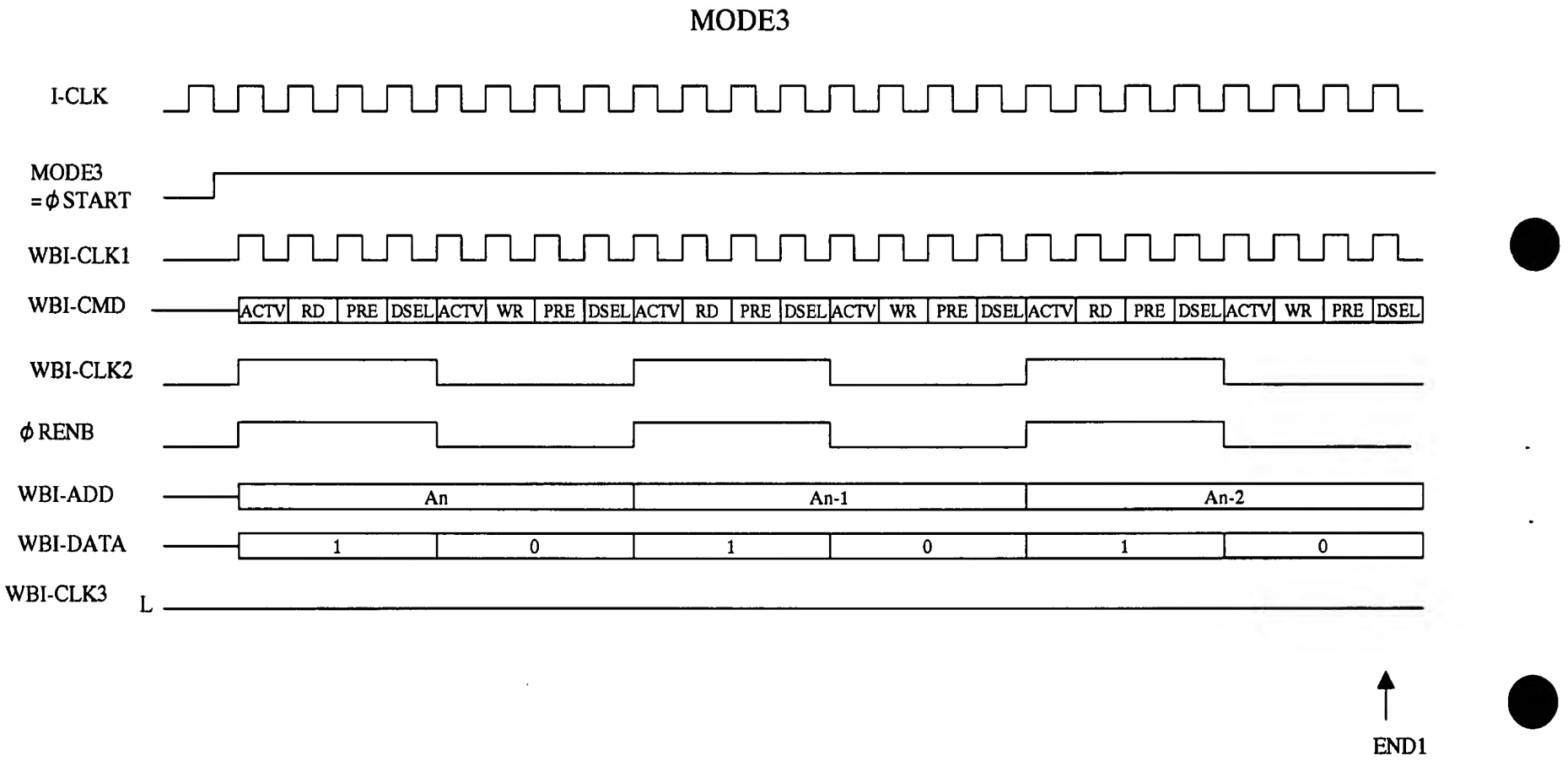
MODE3
I-CLK
MODE3
=φSTART
WBI-CLK1
WBI-CMD
ACTV RD PRE DSEL ACTV WR PRE DSEL ACTV RD PRE DSEL ACTV WR PRE DSEL ACTV RD PRE DSEL ACTV WR PRE DSEL
WBI-CLK2
φRENB
WBI-ADD
An
An-1
An-2
WBI-DATA
1 0 1 0 1 0
WBI-CLK3
L
END1

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FIG. 10

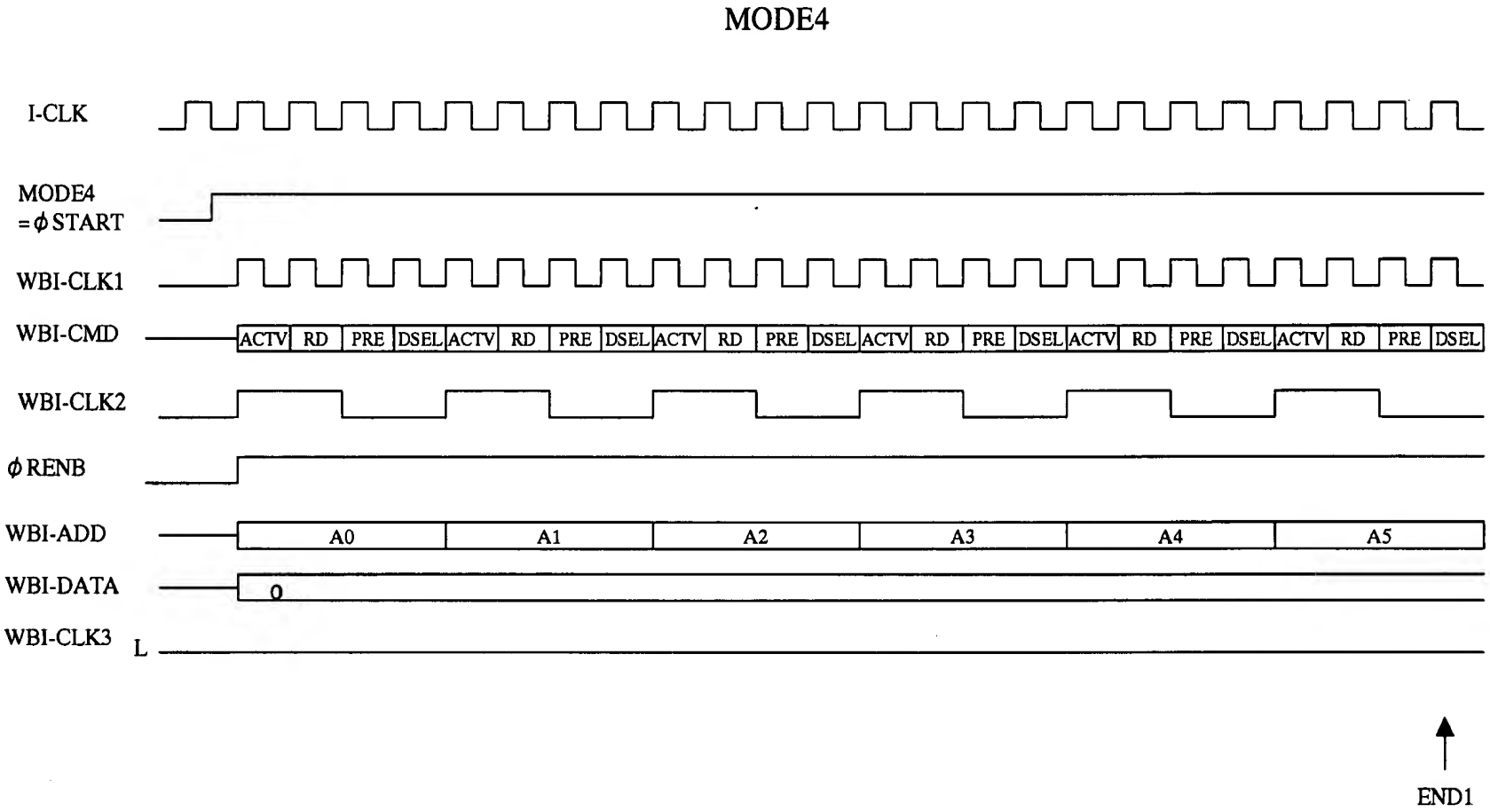

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FIG. 11

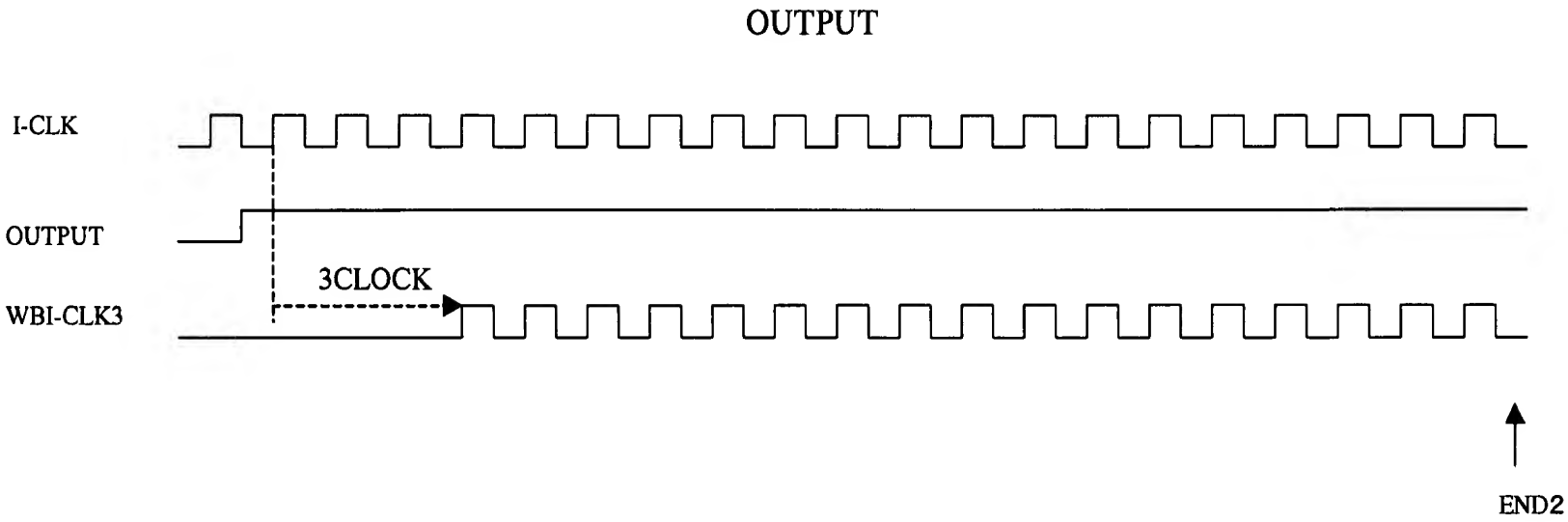


FIG. 12

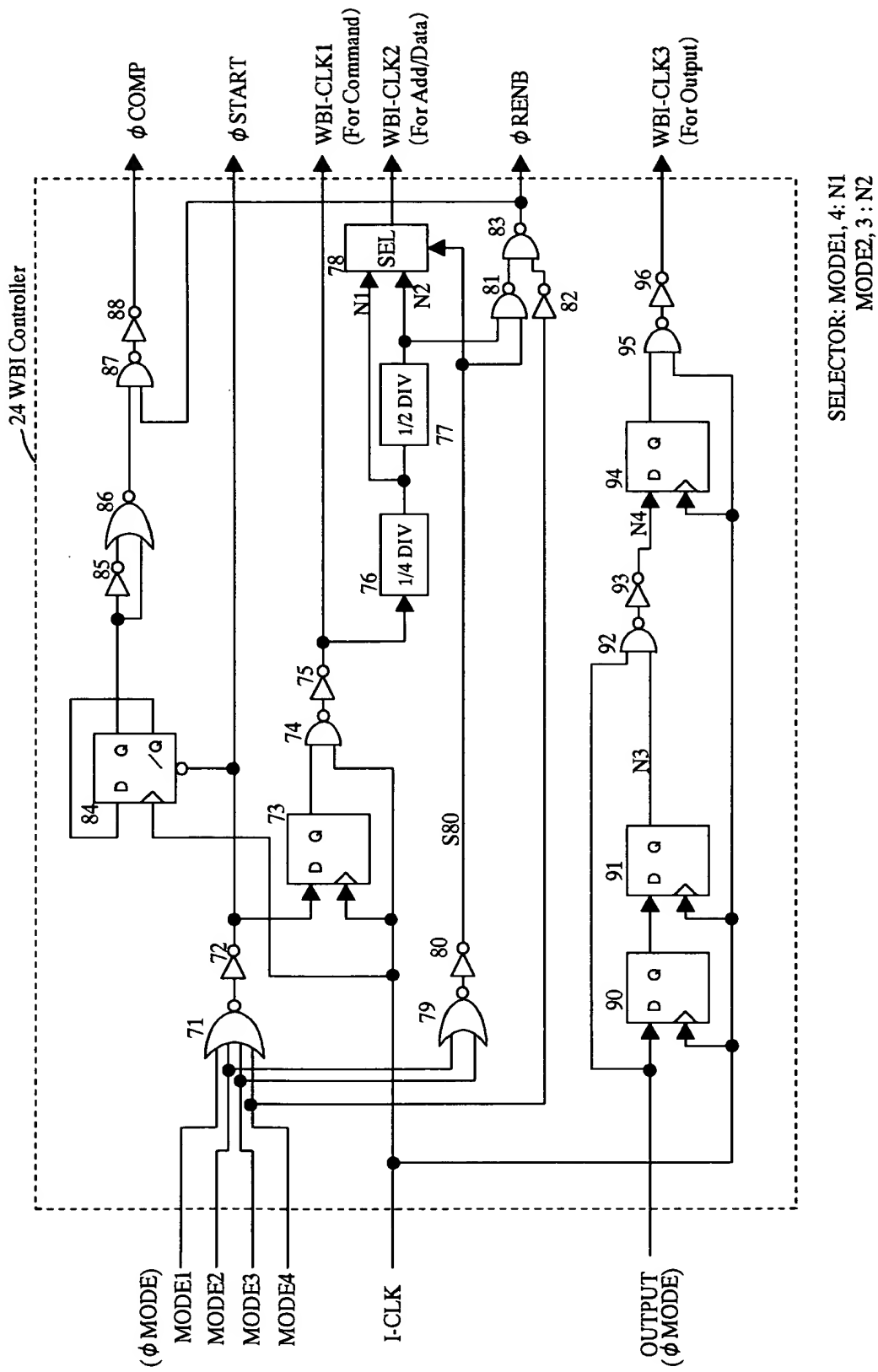

24 WBI Controller
φ COMP
φ START
WBI-CLK1 (For Command)
WBI-CLK2 (For Add/Data)
φ RENB
WBI-CLK3 (For Output)
SEL
1/2 DIV
1/4 DIV
S80
N1
N2
N3
N4
(φ MODE)
MODE1
MODE2
MODE3
MODE4
I-CLK
OUTPUT (φ MODE)
SELECTOR: MODE1, 4: N1
MODE2, 3 : N2

FIG. 13

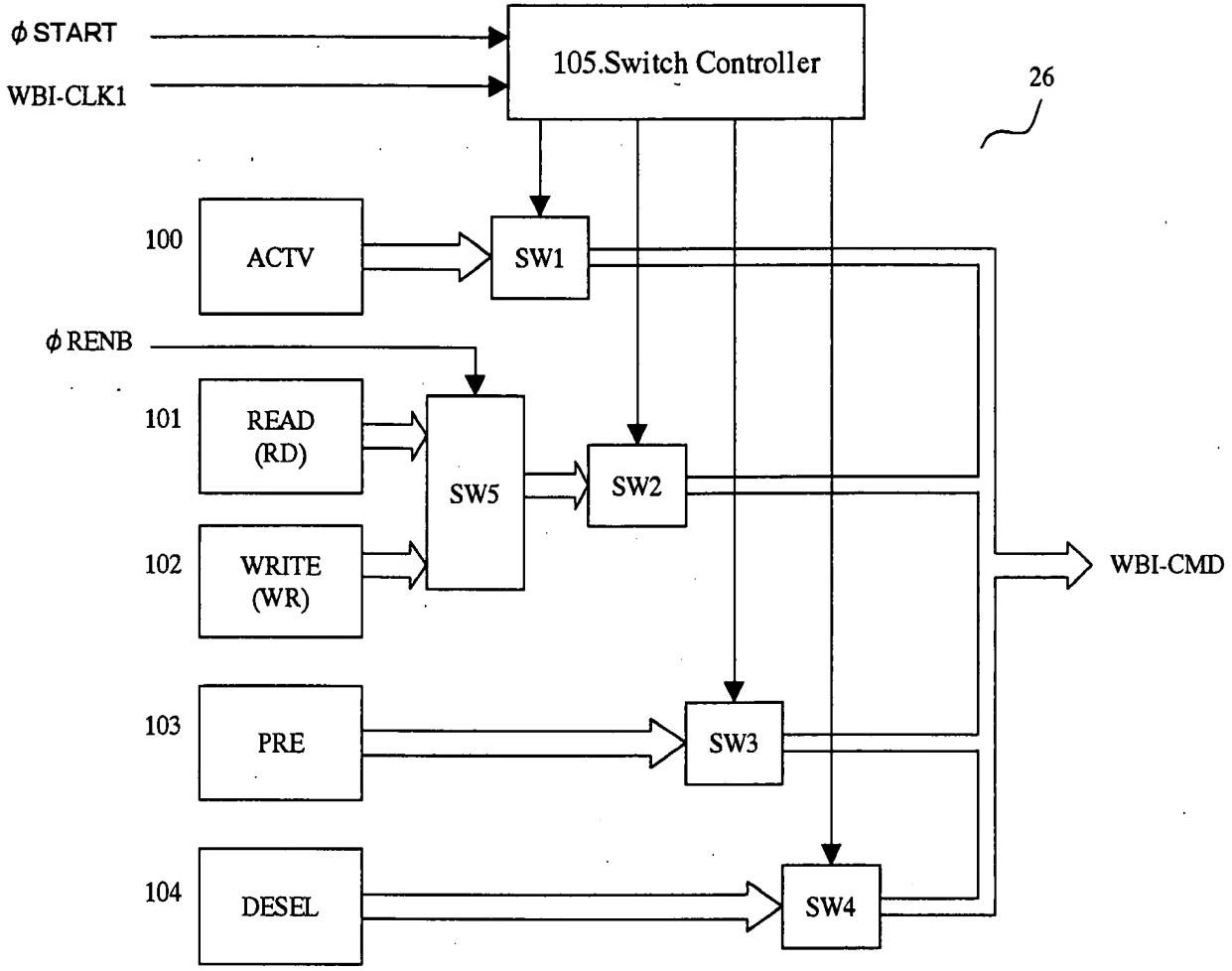
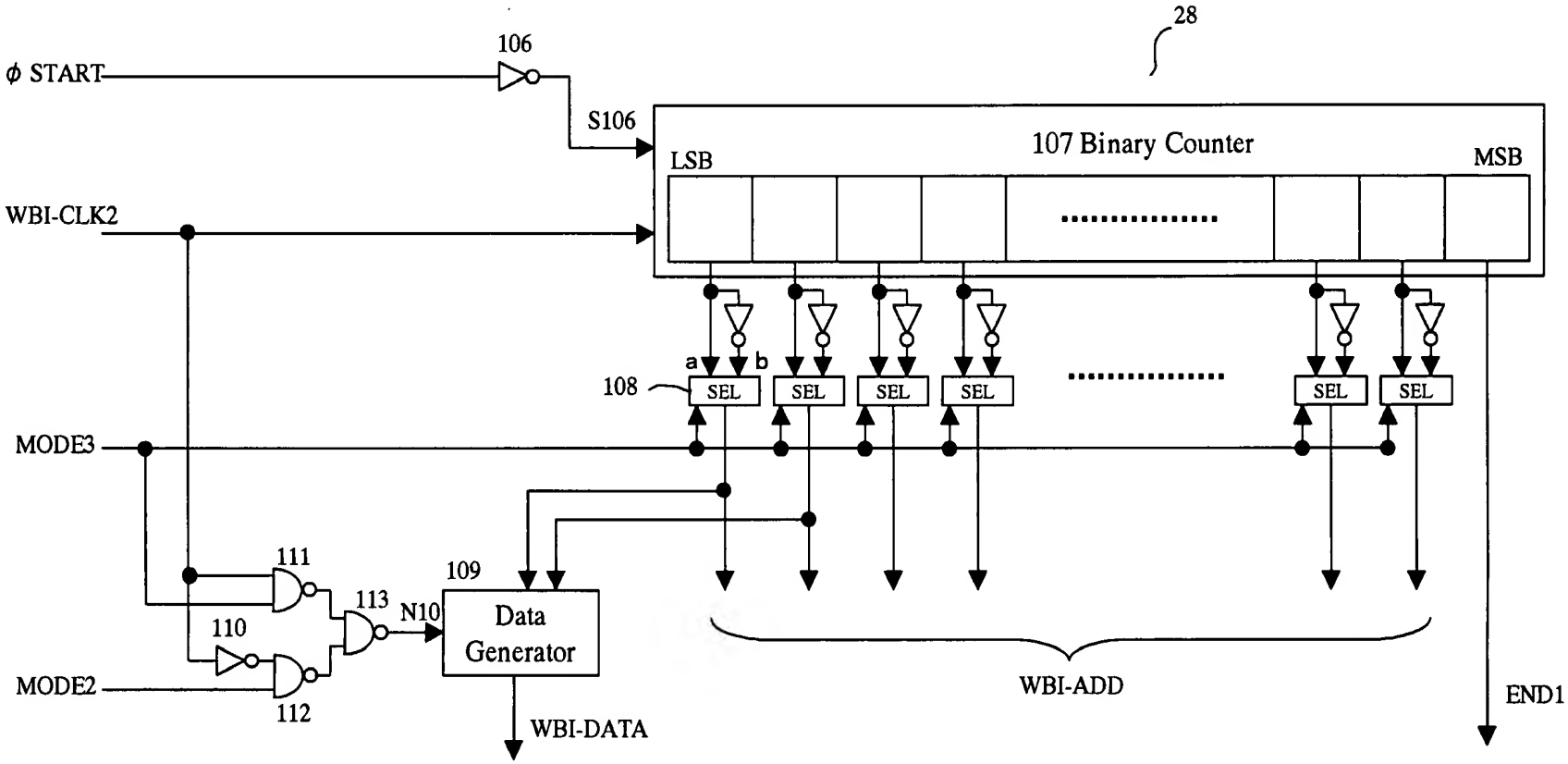

φ START
WBI-CLK1
105.Switch Controller
26
100
ACTV
SW1
φ RENB
101
READ
(RD)
SW5
SW2
102
WRITE
(WR)
WBI-CMD
103
PRE
SW3
104
DESEL
SW4

FIG. 14



SELECTOR: Address Increment : a

Address Decrement : b

FIG. 15A

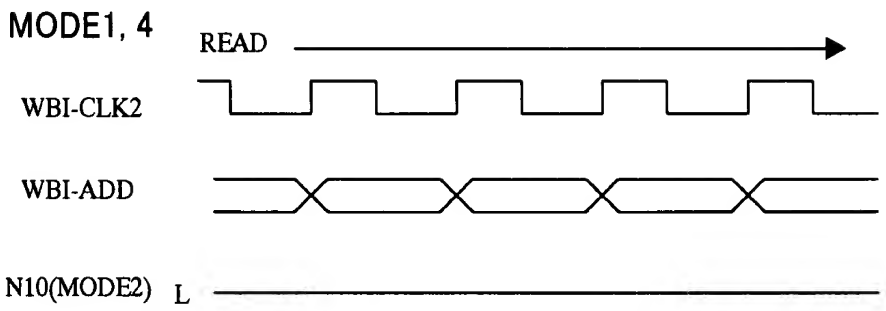


FIG. 15B

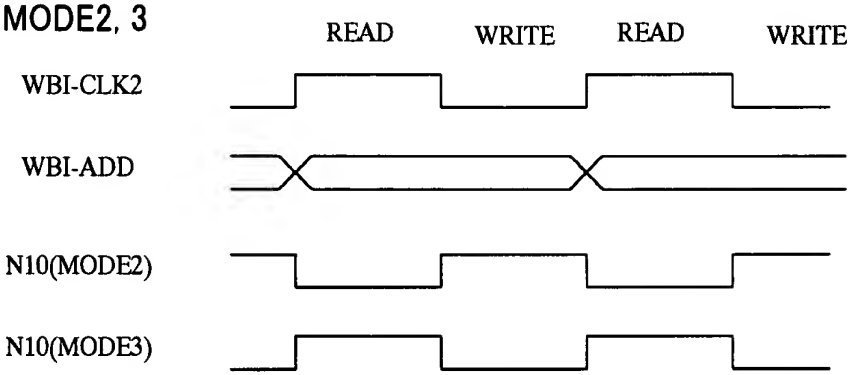


FIG. 15C

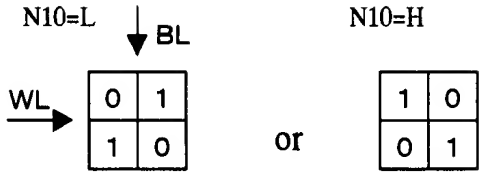


FIG. 16

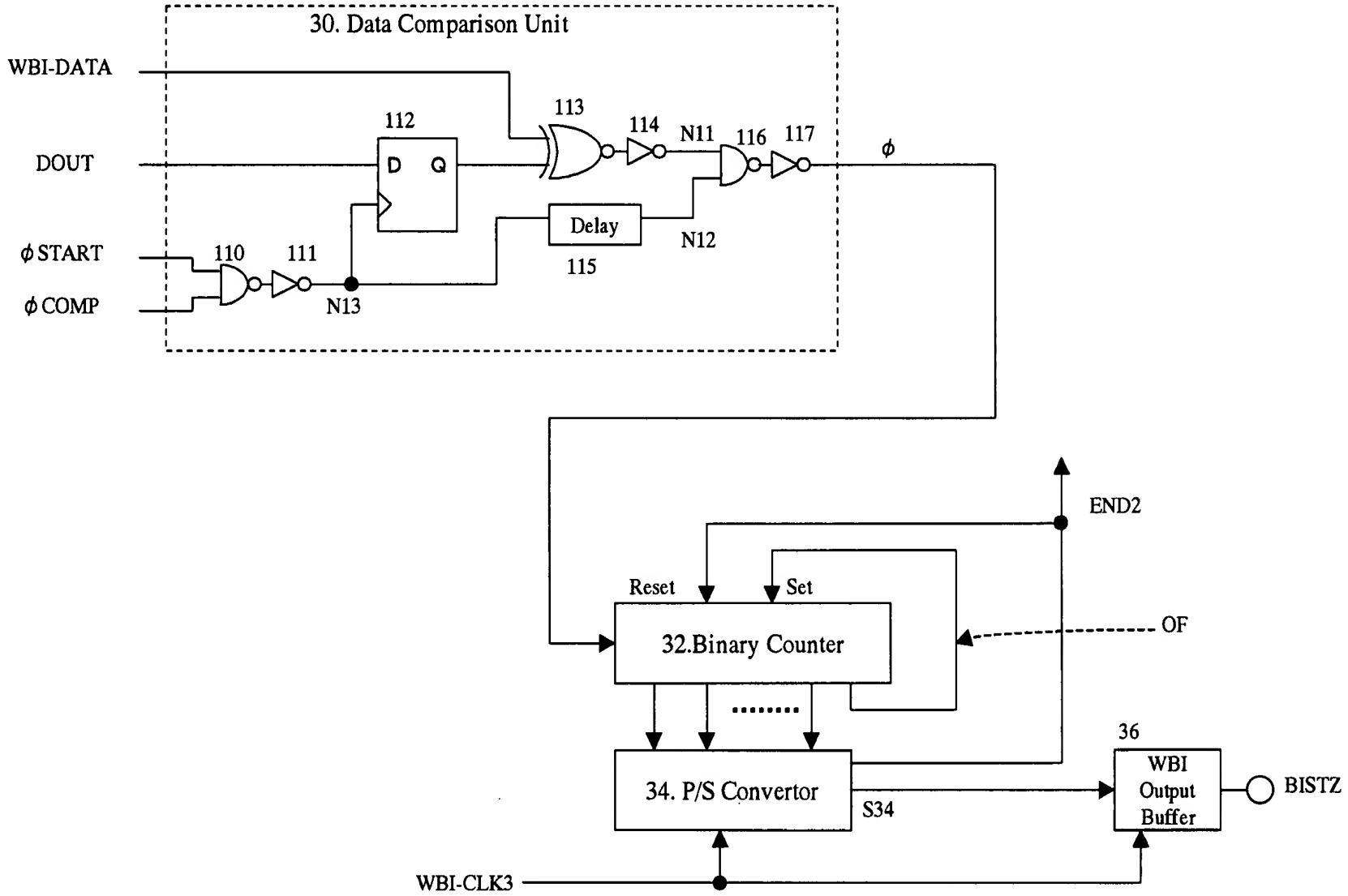

30. Data Comparison Unit
WBI-DATA
DOUT
φ START
φ COMP
112
D
Q
113
114
N11
116
117
φ
110
111
N13
Delay
115
N12
END2
Reset
Set
32.Binary Counter
OF
36
34. P/S Convertor
S34
WBI
Output
Buffer
BISTZ
WBI-CLK3

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FIG. 17

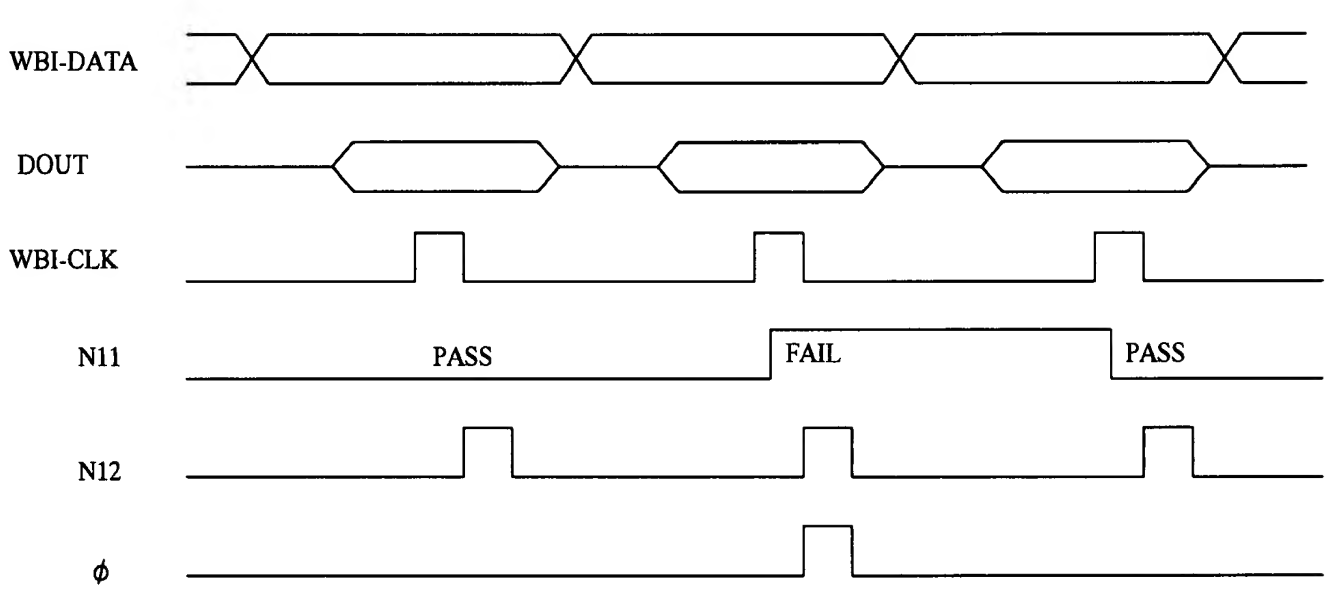


FIG. 18

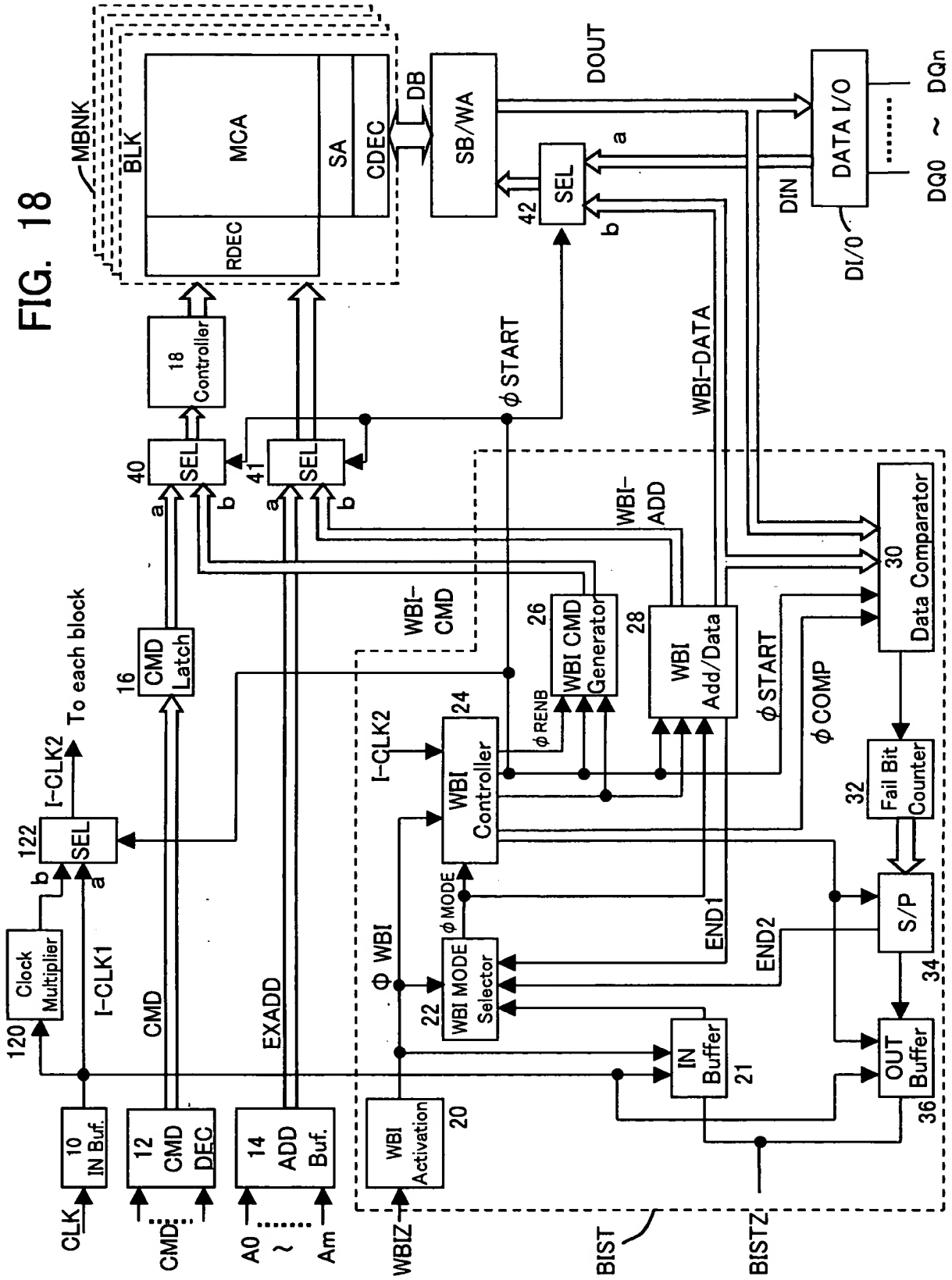

MBNK
BLK
MCA
SA
CDEC
RDEC
DB
SB/WA
DOUT
DATA I/O
DQ0 ~ DQn
DIN
DI/0
SEL
42
18 Controller
40
41
φ START
WBI-DATA
WBI-ADD
WBI-CMD
26 WBI CMD Generator
28 WBI Add/Data
30 Data Comparator
φ START
φ COMP
φ RENB
16 CMD Latch
To each block
I-CLK2
122
24 WBI Controller
32 Fail Bit Counter
S/P
34
φ MODE
END1
END2
120 Clock Multiplier
I-CLK1
CMD
EXADD
φ WBI
22 WBI MODE Selector
IN Buffer
21
OUT Buffer
36
10 IN Buf.
12 CMD DEC
14 ADD Buf.
WBI Activation
20
CLK
CMD
A0 ~ Am
WBIZ
BIST
BISTZ

FIG. 19

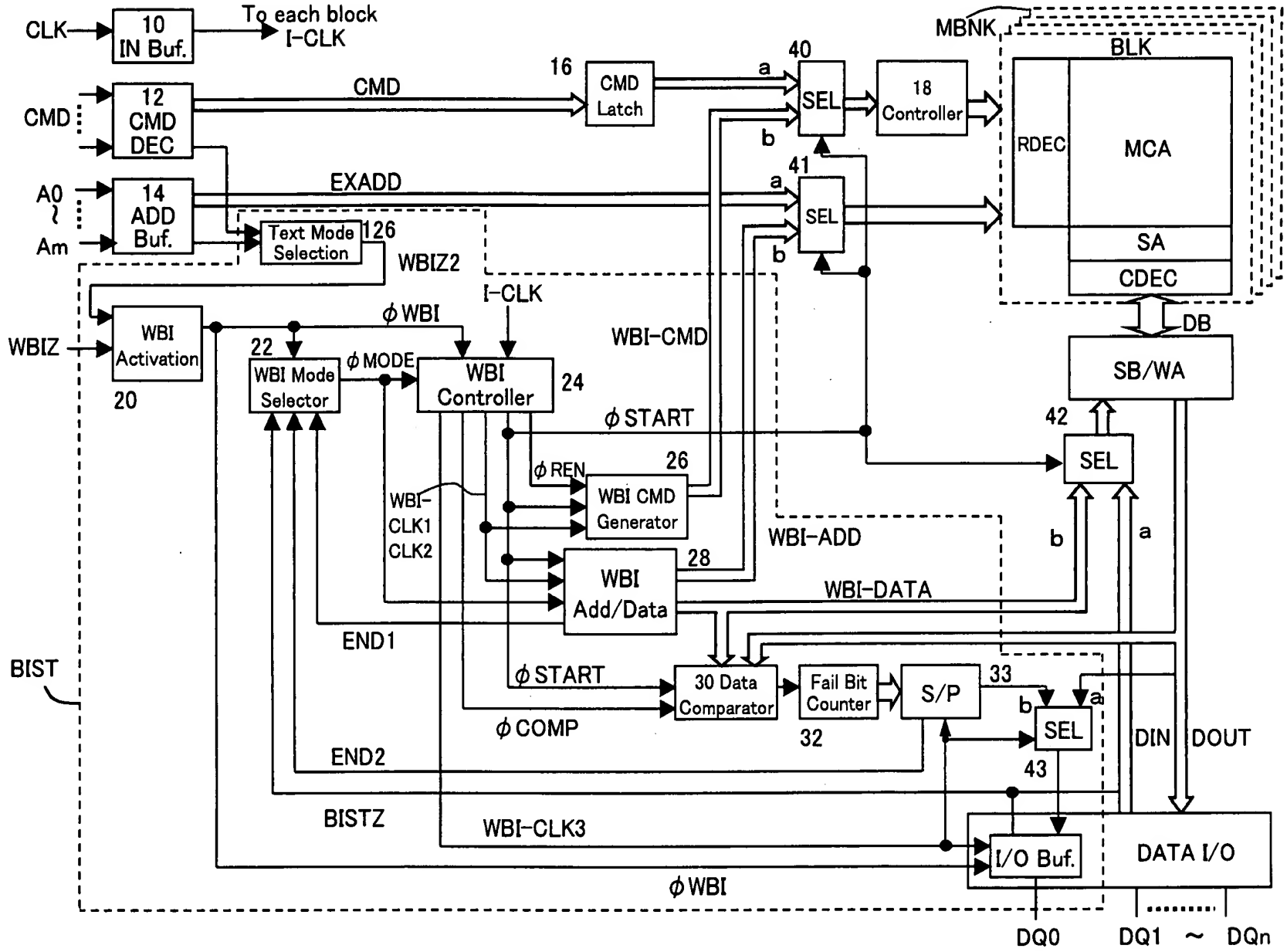
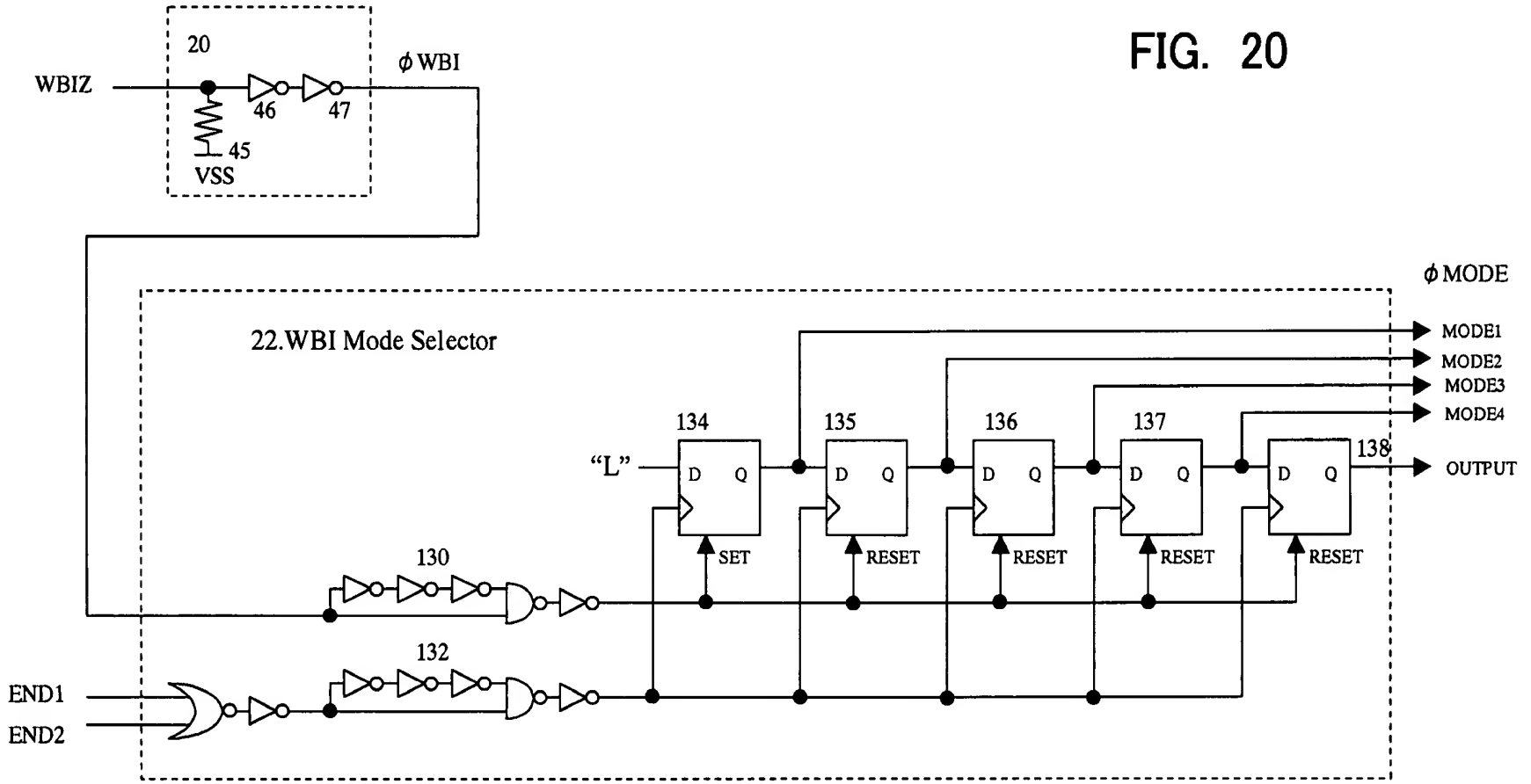

CLK
10 IN Buf.
To each block I-CLK
CMD
12 CMD DEC
16
CMD Latch
40
SEL
18 Controller
MBNK
BLK
RDEC
MCA
SA
CDEC
A0
Am
14 ADD Buf.
EXADD
41
Text Mode Selection
126
WBIZ2
WBIZ
WBI Activation
20
I-CLK
φWBI
WBI-CMD
22
WBI Mode Selector
φMODE
WBI Controller
24
φSTART
DB
SB/WA
42
φREN
26
WBI CMD Generator
WBI-CLK1 CLK2
WBI-ADD
28
WBI Add/Data
WBI-DATA
END1
BIST
30 Data Comparator
Fail Bit Counter
32
S/P
33
DIN
DOUT
φCOMP
END2
43
BISTZ
WBI-CLK3
I/O Buf.
DATA I/O
DQ0
DQ1 ~ DQn

FIG. 20



Q="H": SET

Q="L" : RESET

FIG. 21A

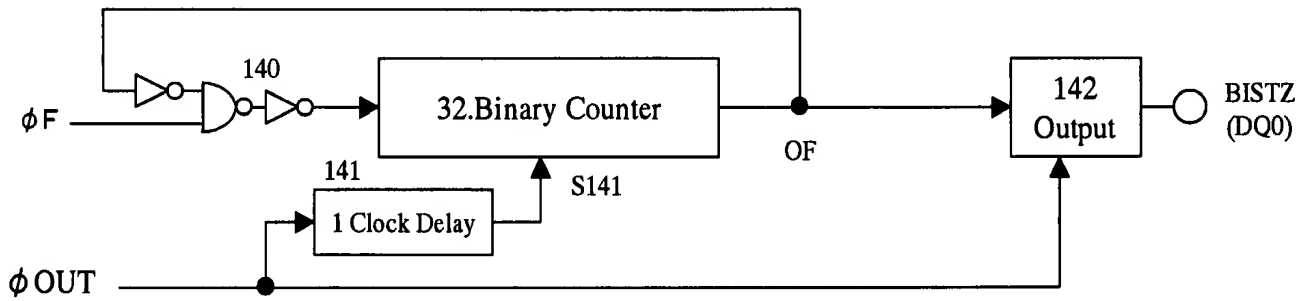


FIG. 21B

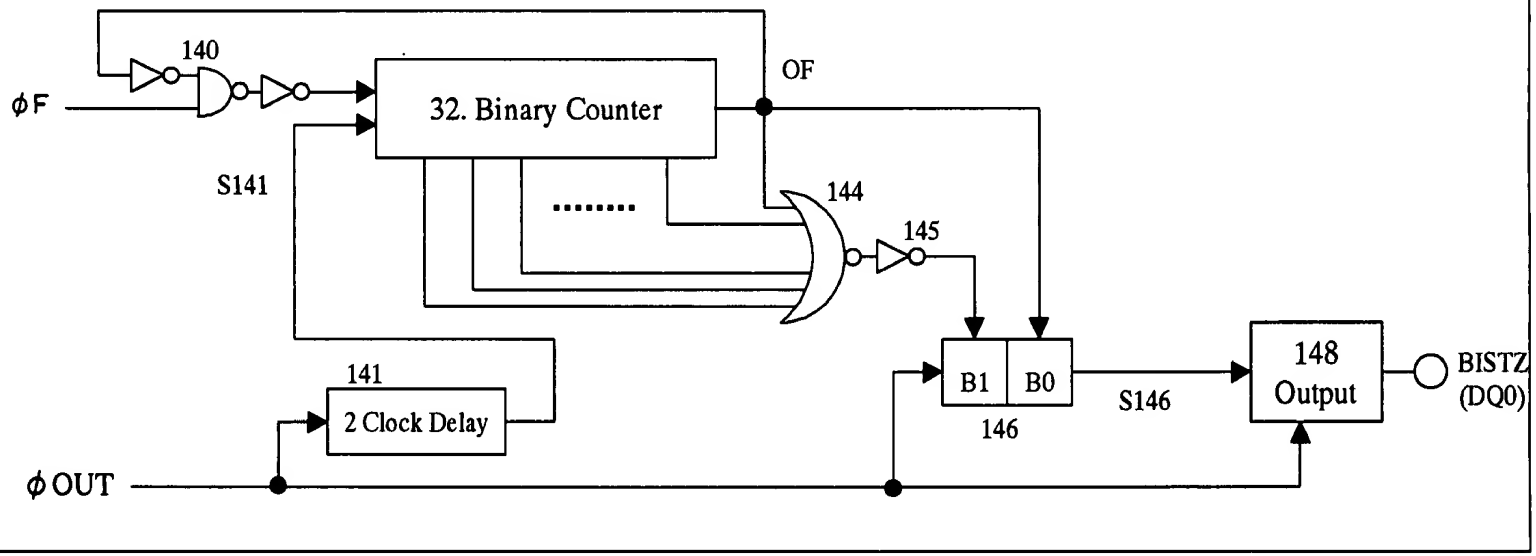


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FIG. 22

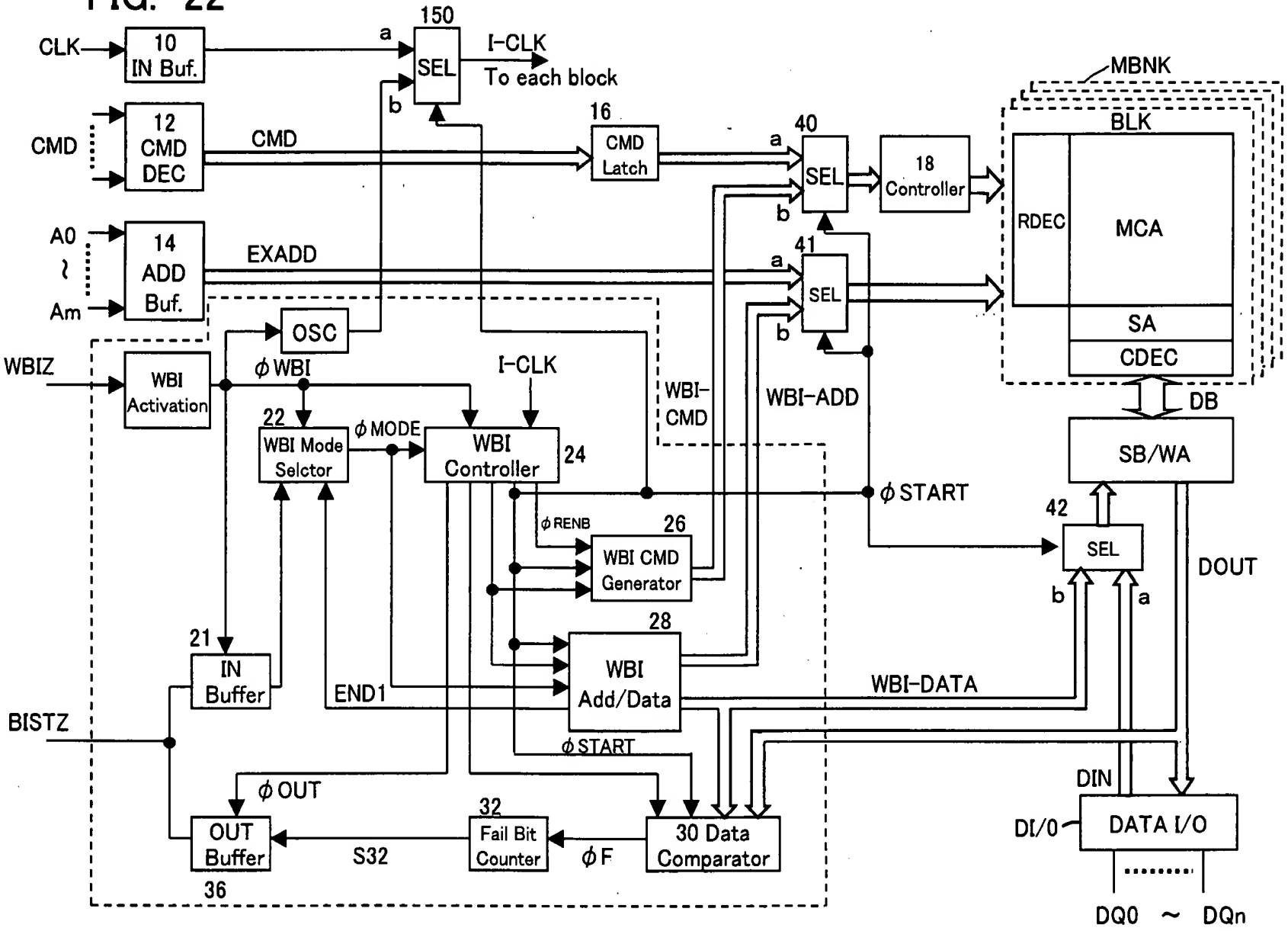

FIG. 23

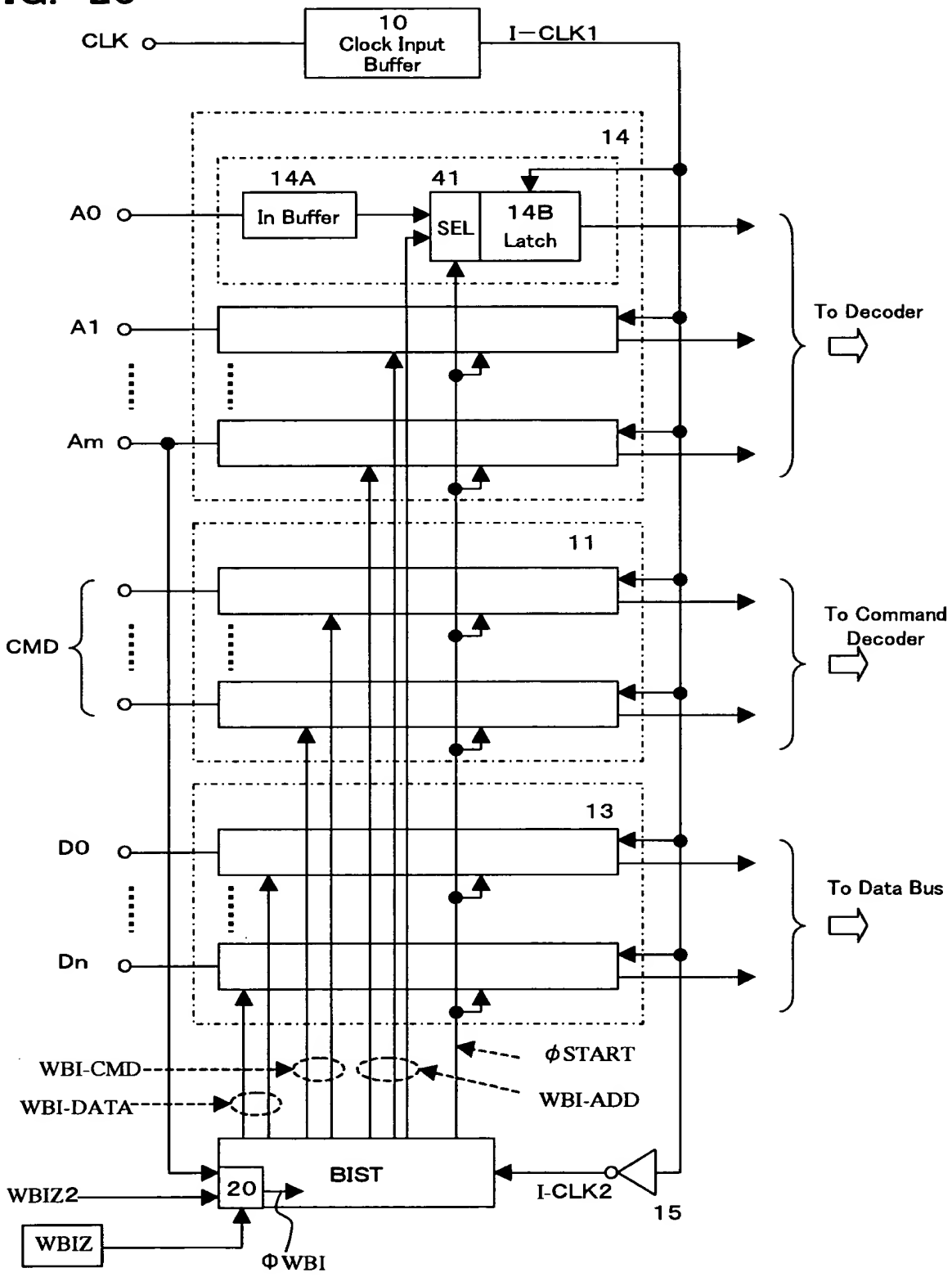
CLK
10
Clock Input Buffer
I-CLK1
14
14A
In Buffer
41
SEL
14B
Latch
A0
A1
Am
To Decoder
11
CMD
To Command Decoder
13
D0
Dn
To Data Bus
WBI-CMD
WBI-DATA
φSTART
WBI-ADD
BIST
20
WBIZ2
WBIZ
ΦWBI
I-CLK2
15

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FIG. 24

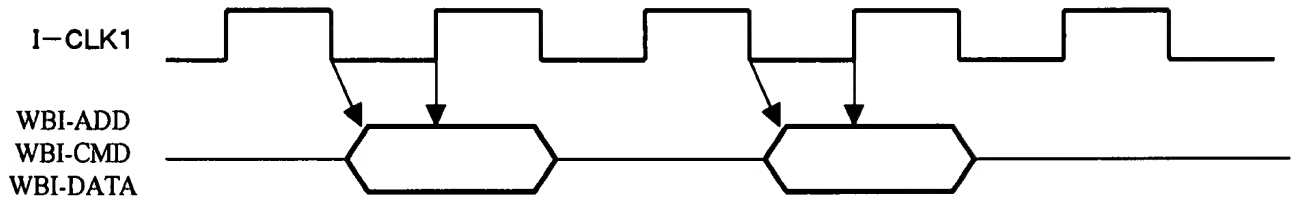


FIG. 25

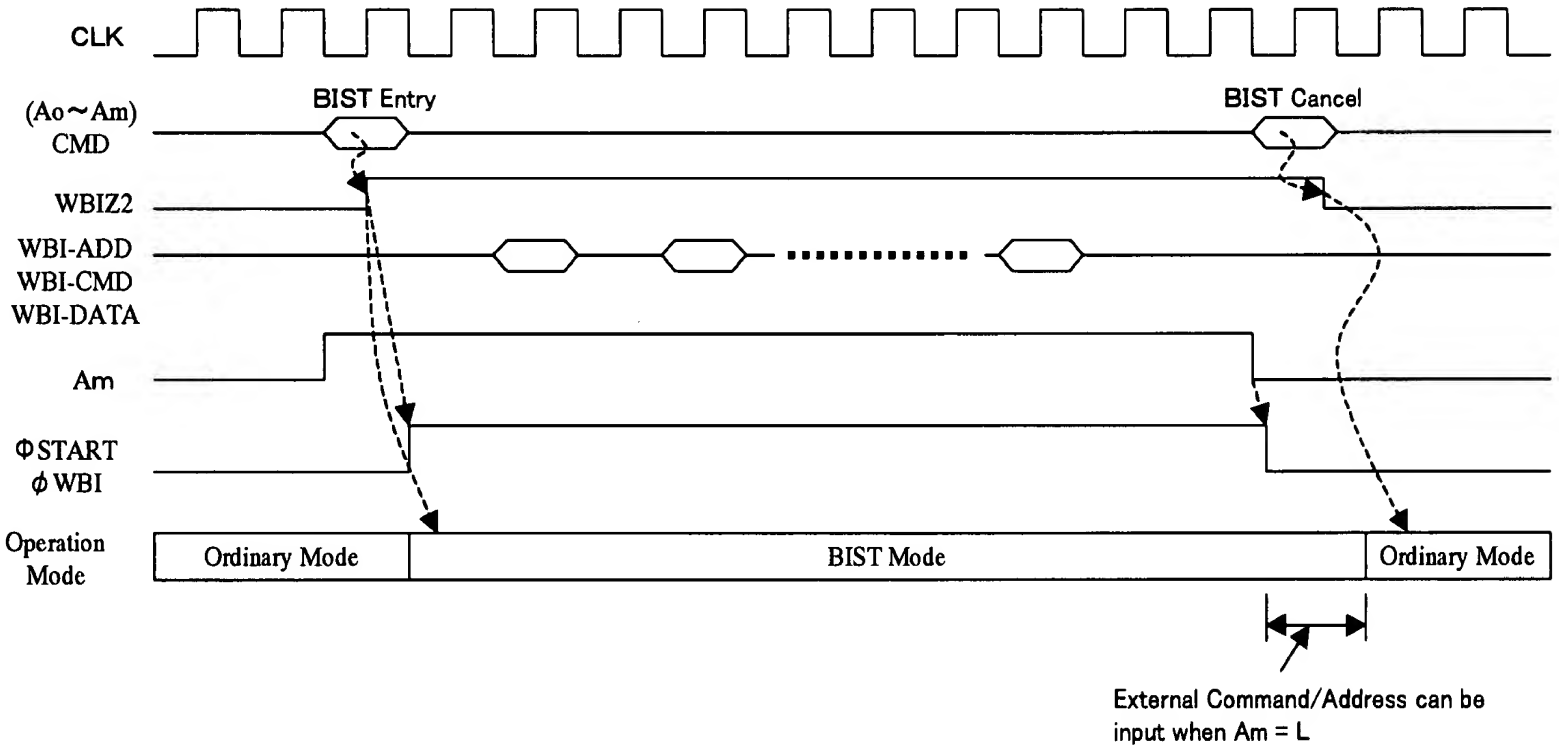

CLK
(Ao~Am)
CMD
BIST Entry
BIST Cancel
WBIZ2
WBI-ADD
WBI-CMD
WBI-DATA
Am
ΦSTART
ϕWBI
Operation
Mode
Ordinary Mode
BIST Mode
Ordinary Mode
External Command/Address can be
input when Am = L

FIG. 26

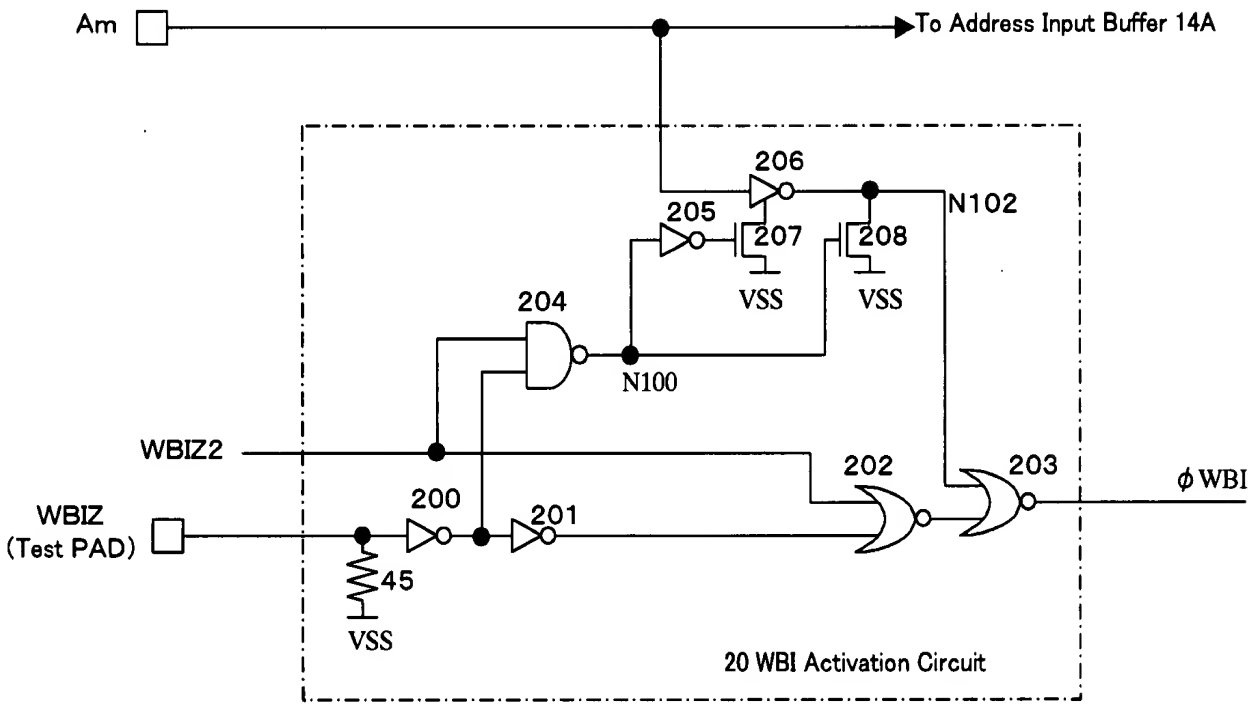
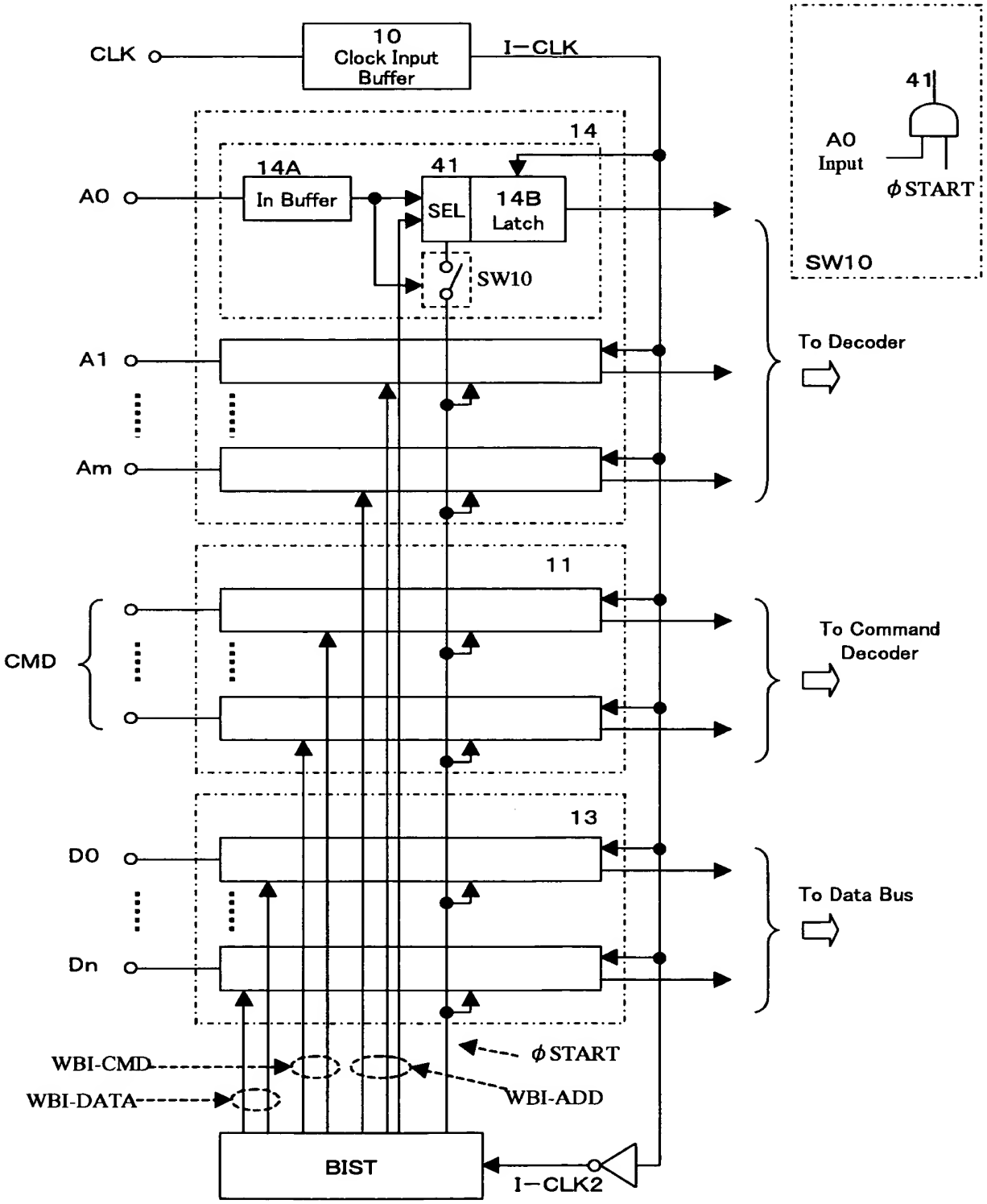

Am
To Address Input Buffer 14A
206
205
207
208
N102
VSS
VSS
204
N100
WBIZ2
202
203
φWBI
WBIZ
(Test PAD)
200
201
45
VSS
20 WBI Activation Circuit

FIG. 27


CLK
10
Clock Input Buffer
I-CLK
14
14A
In Buffer
41
SEL
14B
Latch
SW10
A0
A1
Am
11
CMD
13
D0
Dn
WBI-CMD
WBI-DATA
φSTART
WBI-ADD
BIST
I-CLK2
41
A0 Input
φSTART
SW10
To Decoder
To Command Decoder
To Data Bus

DOCTOR STT6960

FIG. 28

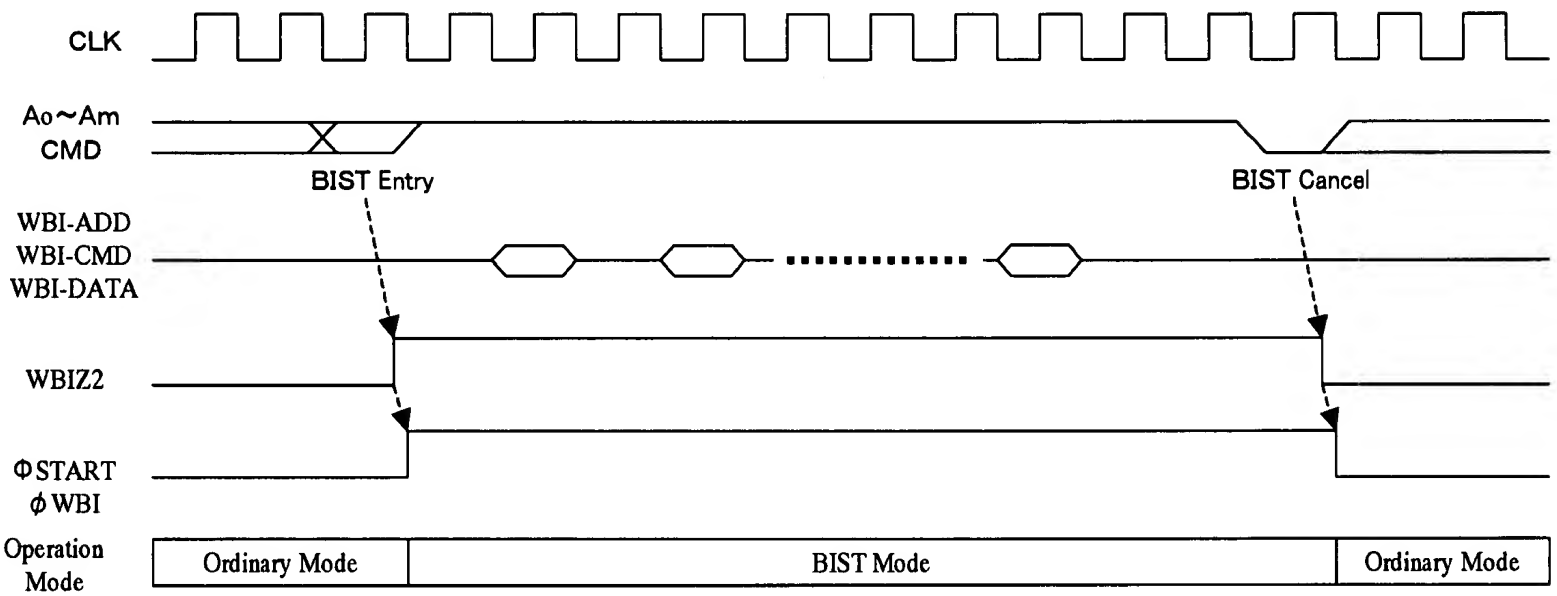


FIG. 29A

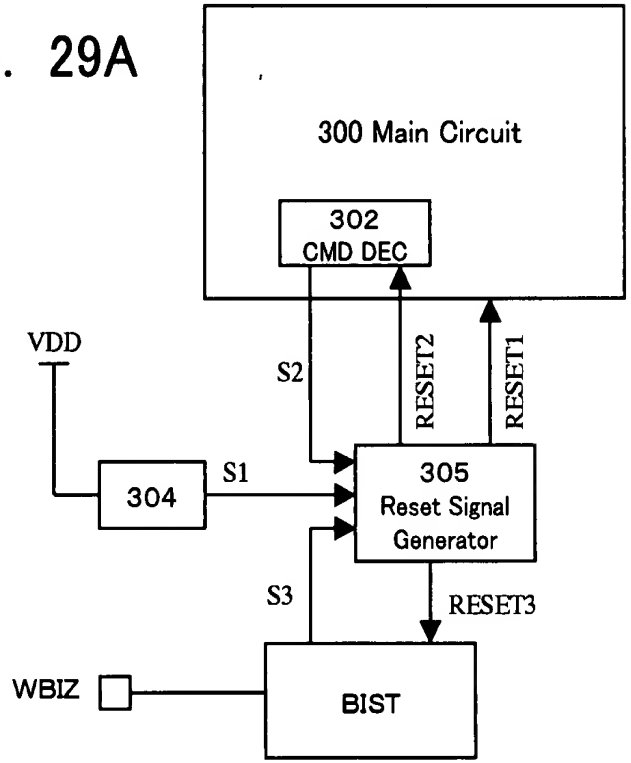


FIG. 29C

	RESET1 (Main)	RESET2 (CMD DEC)	RESET3 (BIST)
S1	○	○	○
S2	○	×	○
S3	○	○	×

○ Reset Signal Generation

FIG. 29B

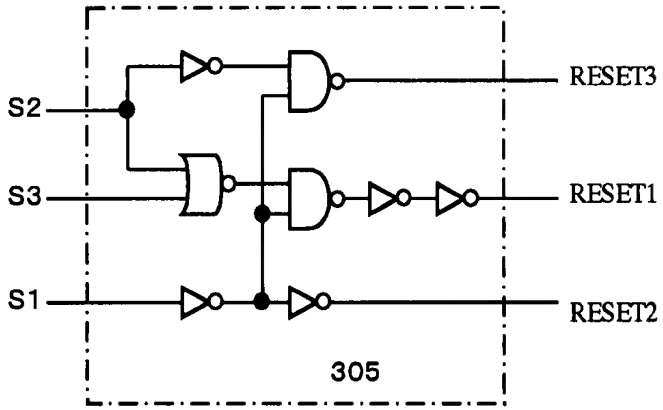
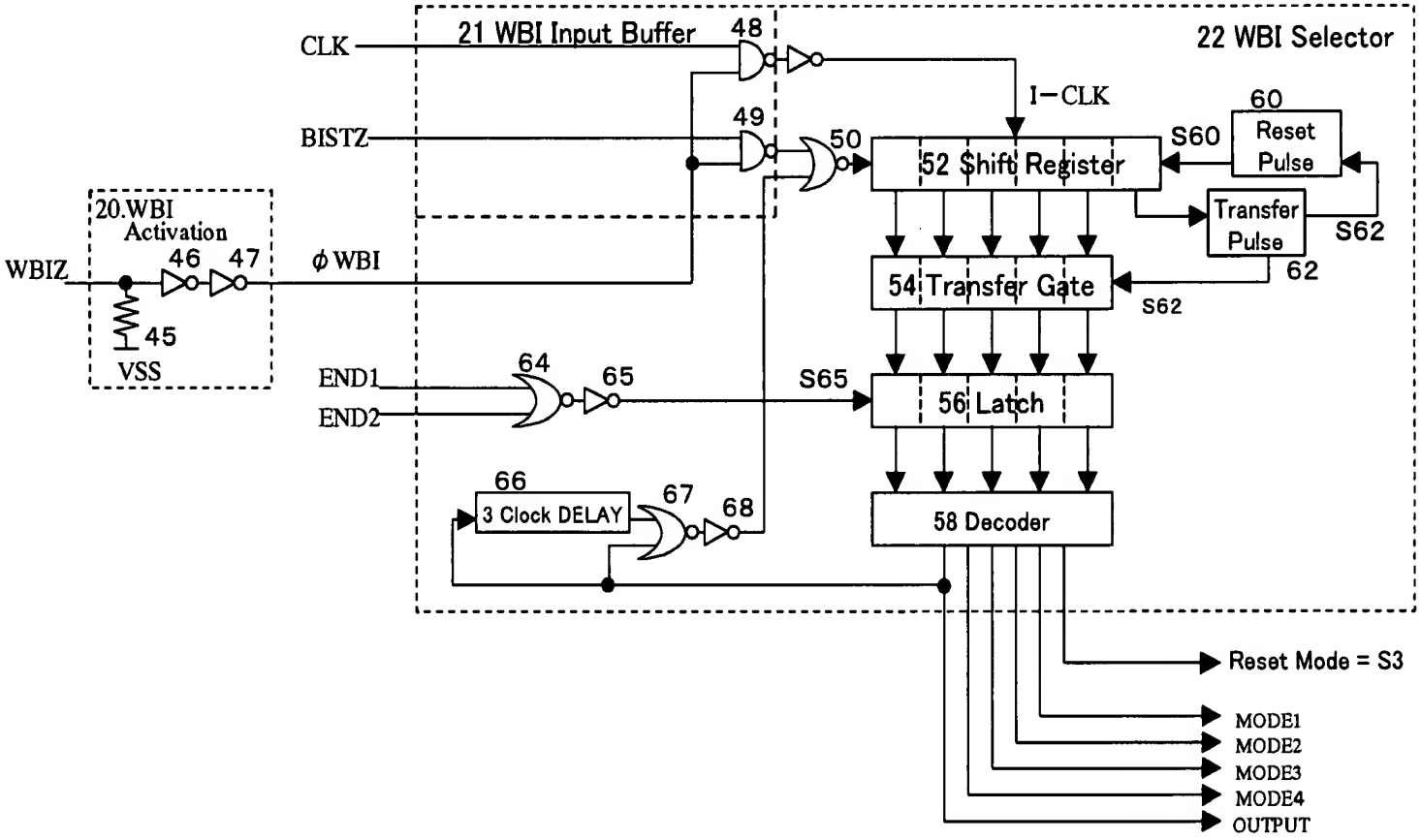


FIG. 30


CLK
21 WBI Input Buffer
48
22 WBI Selector
I-CLK
BISTZ
49
50
52 Shift Register
S60
60
Reset Pulse
Transfer Pulse
S62
62
20.WBI Activation
WBIZ
46
47
φWBI
54 Transfer Gate
S62
45
VSS
END1
END2
64
65
S65
56 Latch
66
3 Clock DELAY
67
68
58 Decoder
Reset Mode = S3
MODE1
MODE2
MODE3
MODE4
OUTPUT